



Setanta  
Space



# Products & AI Solutions

to help your space missions fly smarter

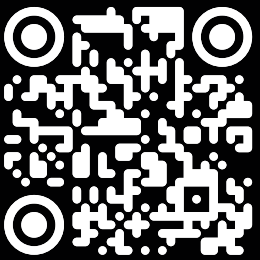


Setanta Space

# Products



See our products in action at  
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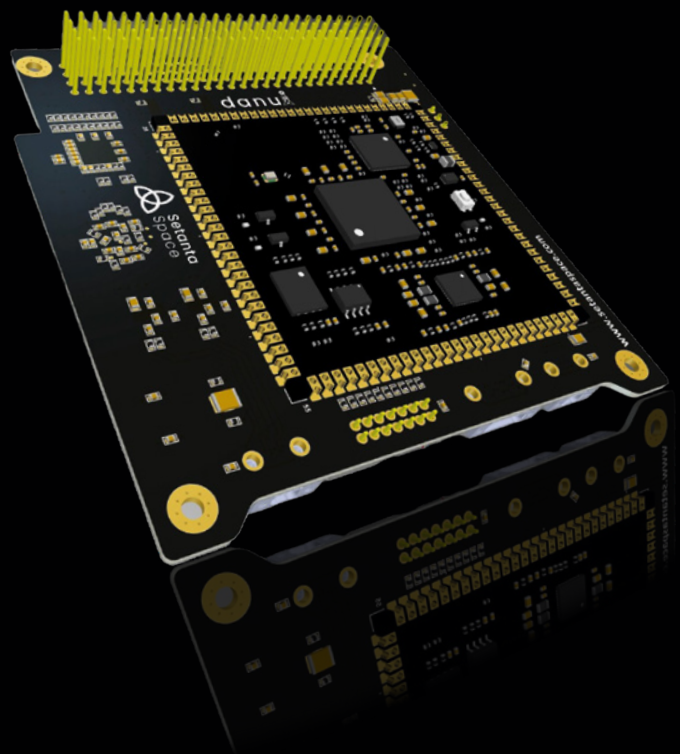


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All our products are available to buy direct  
from our website. Just visit us online at  
[setantaspace.com](https://setantaspace.com).





**Danu** is a modular onboard computer platform designed for small satellites, hosted payloads, and autonomous space systems. Built around the flight proven Microchip SAMV71 architecture and a high-performance FPGA fabric, DANU delivers a flexible balance of reliability, performance, and expandability.



The platform supports **COTS**, **radiation-tolerant**, and **radiation-hard** configurations, enabling a common software and hardware baseline from early prototyping through flight deployment. A modular space tile interface allows DANU to scale from a traditional OBC to a heterogeneous compute node capable of hosting AI accelerators, FPGAs or mission-specific processing.

### Key features

- Modular OBC architecture with optional compute expansion
- SAMV71 / SAMV71RT / SAMRH71 ARM Cortex-M7 processing
- Integrated FPGA for real-time processing, I/O bridging, and reconfigurable logic
- Single-slot spacecraft form factor
- Common software stack across COTS, RT, and RH variants
- Designed for AI, autonomy, and high data-rate payload handling
- Available in PC104, VPX and custom form factors



## System Architecture

### Main Processor

- **Processor Family:** Microchip SAMV71 / SAMV71RT / SAMRH71
- **Core:** ARM Cortex-M7
- **Clock Speed:** Up to 300 MHz (100 MHz for SAMRH71)
- **Architecture:** Deterministic real-time MCU suitable for FDIR and control tasks

The SAMV71 provides a flight-proven microcontroller platform with strong real-time performance, low power consumption, and extensive peripheral support.

### Memory

- On-chip MCU SRAM and Flash
- External memory support (eMMC and MRAM)
- FPGA configuration memory

### Space Tile Concept

- True modularity for spacecraft computing through standardized, swappable computing tiles
- Packages complex subsystems into a single module:
  - FPGA logic
  - AI accelerators
  - Control and management logic
  - Power conditioning
  - Clocking and timing
  - Configuration and system interfaces
  - Mass Memory
- Dramatically reduces hardware development time and system integration effort
- Simplifies avionics architecture by replacing custom boards with proven computing blocks
- Enables rapid mission reconfiguration without redesigning the full avionics stack
- Allows capabilities to be upgraded or changed late in the mission design cycle
- Provides a scalable path from early prototypes to flight systems

## Variants

### DANU

- Integrated SAMV71 /SAMV71RT / SAMRH71 MCU
- Integrated space tile
- Optimized for:
  - CubeSat OBCs
  - Payloads
- Specifically aimed at LEO, Aerospace and Defence

### DANU RH

- SAMRH71 radiation-hard MCU
- Integrated space tile
- Suitable for:
  - Advanced payload handling
  - Onboard autonomy
  - AI pre-processing and inference
- Designed for:
  - Long-duration missions
  - Higher radiation environments
  - Exploration and deep-space platforms
- Total Ionizing Dose (TID): > 100 kRad (Si) accumulated tolerance. Also immune to SEL up to ~62 MeV·cm<sup>2</sup>/mg

### DANU RT

- SAMV71 MCU
- Integrated space tile
- Suitable for:
  - Advanced payload handling
  - Onboard autonomy
  - AI pre-processing and inference
- Designed for:
  - High reliability
  - Short to medium duration missions
  - Low to medium radiation environments
  - Satellites in orbit
- Total Ionizing Dose (TID): ~30 kRad (Si) accumulated dose tolerance. Latch-up: Immune to single-event latch-up (SEL) up to ~62 MeV·cm<sup>2</sup>/mg

## Interfaces

### Communications

- Ethernet
- SpaceWire
- CAN / CAN-FD
- UART
- SPI
- I<sup>2</sup>C
- GPIO

### Expansion

- Modular space tiles for:
  - AI accelerators
  - Co-processors
  - Custom mission hardware

## Software Support

DANU's flight software is built using a component-based flight software kit, combining an extensive library of validated onboard software components with a lightweight service-oriented framework. This approach promotes portability and modularity across COTS, RT, and RH MCU variants, while supporting deployment on both the DANU hardware and desktop environments for early prototyping.

Standardized service interfaces are used to assemble mission-specific stacks for data handling, monitoring, automation, and communications, allowing protocols and subsystems to be swapped or emulated without impacting higher-level behaviour. Platform abstraction enables the same software model to run on operating systems from Linux to hard real-time environments such as FreeRTOS or RTEMS, with peripheral access provided through reusable library components.

Graphical and command-line tooling support configuration, code generation, build and test, integrating with common development environments, and automation pipelines. The same tooling underpins ground-like interaction and automated test scripting, enabling iterative, agile development of mission-specific flight software for DANU.

### Applications

- CubeSat and SmallSat OBC
- AI-enabled Earth observation
- Space Situational Awareness
- Autonomous navigation and GNC support
- Payload control and data handling
- Technology demonstration missions
- Aerospace and Defence

### Electrical & Mechanical (Summary)

- **Form Factor:** Single-slot PC/104 modular spacecraft board, VPX, and custom form factors
- **Radiation:** COTS, RT, and RH options available

Detailed electrical and mechanical specifications are available upon request.

**DANU is designed as a long-lived platform, not a single-mission board. Its modularity, scalability, and common software baseline allow missions to scale capability without redesigning the core OBC, reducing non-recurring engineering costs, qualification and program risk.**

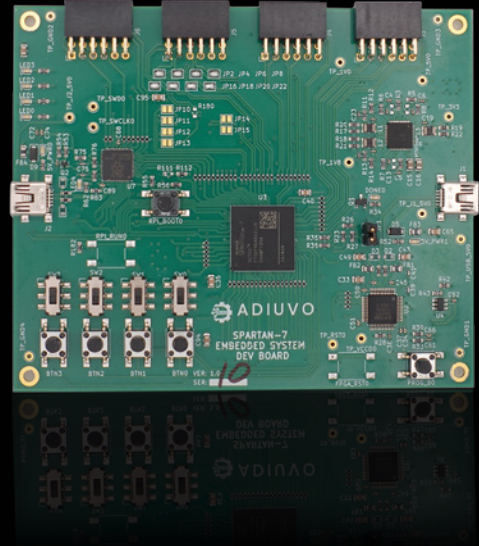
DANU is available as a standard product or as a mission-customized configuration. Space tiles and software stacks can be provided to meet specific mission needs.

For detailed specifications, radiation reports, or integration discussions, contact the Setanta Space team.



# astria BOARD

The **Astria & RPI 2040** is designed to support a range of developments from simple logic and embedded system development, to more complex solutions such as image processing.



## Key features

- AMD Spartan 7 XC7S6 with 6,000 logic cells, 5 BRAM, 2 CMT, 10 DSP48
- Raspberry PI RP2040 processor providing dual-core Arm Cortex-M0+ processor running at 133 MHz
- FTDI232H - For JTAG Programming
- SDRAM - 64 Mbit
- 4 Pmod - Three for FPGA, one for RPi 2040 - Ability to fit high speed LVDS transceiver on one FPGA Pmod
- User Flash - connected to FPGA 32 Mbit QSPI
- FPGA Configuration PROM 256MBit
- Four User LEDs
- Four push button switches
- Four SPST switches
- 100 MHz Reference clock

## Application examples include:

- **RPI\_FPGA\_UART\_AXI** *Vivado 2023.2* Configures a UART in the RP2040 to communicate with the FPGA, sending a protocol over the UART and IP in the FPGA AXI peripherals can be accessed and controlled. In this version three AXI GPIO are connected to three LEDs, the final LED is connected to an AXI timer to demonstrate PWM on the LED. The 4 slide switches are also connected to the AXI GPIO to enable their status to be read over the AXI GPIO.
- **SDRAM** *Vivado 2023.2* - SDRAM example for the SDRAM on the board.
- **MBV\_MCS** *Vivado & Vitis 2024.1* MicroBlaze V (RISC-V) MicroController System implemented on the Spartan 7.
- **S7\_LEO** *Vivado 2023.2* IO check of all FPGA PMOD IO and 4 LED, walks an LED around all 28 LEDs (4 on board, 24 on Pmod LED - not included) - also connects through the user flash to the RPI for testing.
- **DELTA\_SIGMA** *Vivado 2024.1* Delta Sigma output at 1KHz on Pmod 1 pin 1, PWM sine output at 1 KHz on Pmod 1 pin 2 - external RC needed for recovery.

## References

Reference Designs, XDC, Schematics, Vivado board definition can be found at

[https://bitbucket.org/adiuvo-engineering/leonidas\\_embedded\\_development/src/main/](https://bitbucket.org/adiuvo-engineering/leonidas_embedded_development/src/main/)

# astria TILE

The **Astria Embedded System Tile** provides developers with a risk-free way of integrating a Spartan 7 in their design without the worry of designing a chip-down solution.



## The tile measures 59 x 59mm and provides:

- Supply voltage 4.5 to 18V
- Spartan 7 XC7S25 with 23,360 Logic Cells, 80 DSP, 45 BRAM
- Configuration Memory 256 Mbit QSPI
- Done LED
- Two user LED
- USB JTAG - Connector needed on carrier board
- 100 MHz Oscillator
- Reset Button
- Boot selection header (JTAG/QSPI)
- PSRAM – 32 Mbit – Serial RAM connected to the FPGA
- 82 I/O including – Power and Ground, JTAG, 32 I/O at 3v3, 41 I/O configurable voltage (3v3-1.2V and LVDS)

## To help get you started, the Astria Embedded System Tile comes with:

- User guide
- Schematic
- Vivado Board definition
- Reference Designs - including IP to enable processor to access FPGA internals using processor UART / SPI
- Tile footprint in Altium to help accelerate your design

*This information is presented on Adiuvo Engineering's public repository and Setanta Space can be contracted to develop your application or assist with it.*

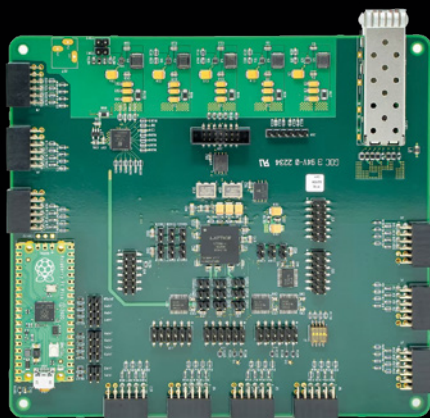
## Typical applications which would benefit from the tile:

- **System Controller** – Power supply sequencing, power monitoring, configuration management, board management and supervision / communication interface.
- **Protocol conversion** – Convert to and from bespoke / legacy protocol.
- **Sensor Aggregation** – Aggregate several different sensor types for easy access by processor
- **I/O expansion** – Provide additional interfaces e.g. QSPI, SPI, I2C etc.
- **Processing offloading** – e.g. Control algorithm such as PID, Filtering, co-processing , encryption / decryption of data streams entering and leaving system.
- **Health and Usage Monitoring systems** – Integrate with sensors e.g. accelerometer, pressure, humidity etc to monitor the environmental operating conditions.
- **Rapid Prototyping** – quickly demonstrate the concept required in an FPGA. Reduces risk of FPGA integration / Removes obsolescence management issues.



# galaxia<sup>®</sup>

## DEVELOPMENT BOARD



The **Galaxia<sup>®</sup> Space Development Board** is intended to support development of demanding space applications, which require low power, high performance and of course a low single event upset rate.

It provides users with a Certus<sup>™</sup>-NX LFD2NX-40 which is the commercial equivalent of the Certus-NX-RT device offered by CAES, and is an excellent platform for the development of applications including:

- Deployment Cameras
- Temperature Control Systems
- Motor and Actuator Control
- Telemetry and Telecommand processing
- Health and Usage Monitoring
- Radiation Beam Testing for design proving
- Implementing Compression algorithms
- Implementing Cryptographic security

### The board provides users with:

- Certus<sup>™</sup>-NX LFD2NX-40
- 80 I/O accessible via Pmod
- 14 ADC Channels – Including ADC Reference
- 128 Mbit NOR flash for configuration
- 256 Kbit MRAM memory
- 100 MHz Oscillator
- Lattice In-System Programmable Hardware Management Expander
- RPi Pico

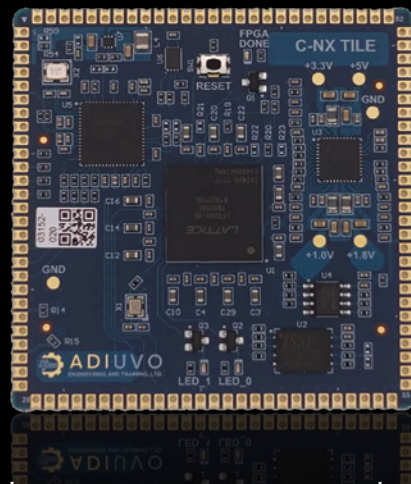
The Lattice Certus<sup>™</sup>-NX FPGA provides the user with 40K LUTs, 2.5 Mbit of BRAM, 56 DSP (18x18), two ADCs and inbuilt 32 KHz and 450 MHz Oscillators.

### Further capabilities

It is also possible to deploy RISC-V processors on this development board, using the Lattice Propel tool. Examples of this can be examined in the tutorials at [adiuvoengineering.com/post/lattice-propel-risc-v-part-one-hardware](https://adiuvoengineering.com/post/lattice-propel-risc-v-part-one-hardware) and [adiuvoengineering.com/post/lattice-propel-risc-v-part-two-software-development](https://adiuvoengineering.com/post/lattice-propel-risc-v-part-two-software-development).

What makes the Galaxia® Space Development Board unique is the provision of the RPi Pico, providing developers with a wide range of capabilities including:

- **Clock Generation** – Generation of up to 65 MHz reference clock using the PIO.
- **Communications emulation** – Emulation of a differential backplane bus.
- **Communications Monitoring** – Monitoring and logging communications.
- **Sensor emulation** – Emulation of sensors across the system and implementation of failure modes.
- **Complex communications creation** – Implementation of a space wire communication protocol between the FPGA and the Pico. This provides a simple interface which can be controlled over the USB communication.
- **Power management and monitoring** – Monitoring the power network, to control, monitor and observe the dissipated power as the FPGA design is used under load or to test, for example, a beam line.



The **Galaxia® Tile** is developed using the same FPGA as the Galaxia® Development Board, enabling it to be designed into missions or more advanced prototyping/testing solutions.

The tile measures 59mm x 59mm and provides developers with:

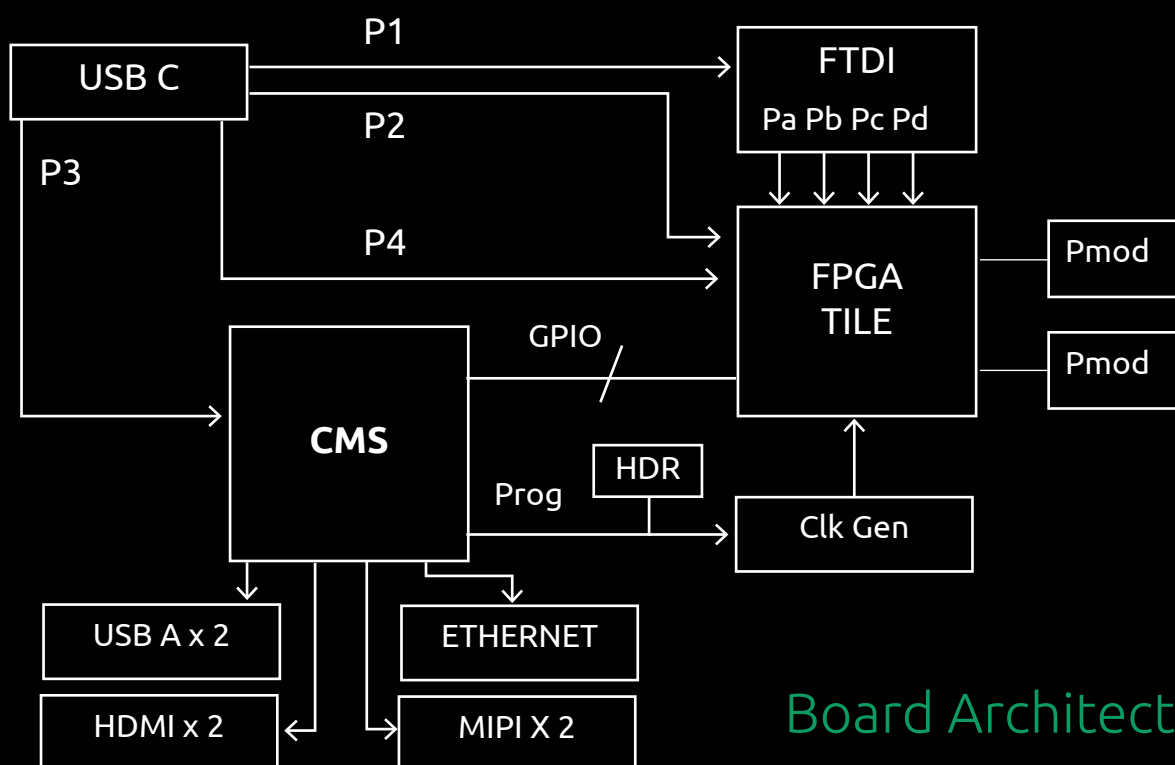
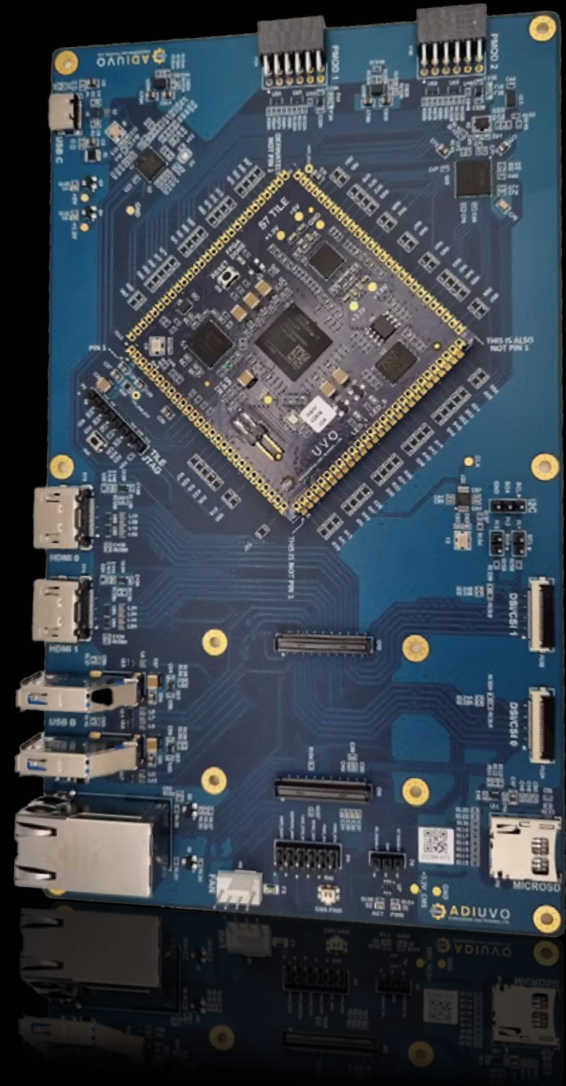
- Single Supply Voltage 4.5V to 18V
- Onboard UART Debug Interface
- Lattice Certus™-NX LFD2NX-40
- Configuration Memory 256 Mbit QSPI
- Done LED and Two user LEDs
- USB JTAG
- USB Connector needed on carrier board
- 100 MHz Oscillator
- Other Global clock pins broken out via I/O
- Reset Button
- PSRAM – 32 Mbit – Serial RAM connected to the FPGA
- 82 I/O including – Power and Ground, JTAG, 32 I/O at 3v3, 41 I/O configurable voltage (3v3-1.2V and LVDS)

# nexus

CARRIER CARD



The **Nexus Carrier Card** takes either Astria or Galaxia tiles, and is designed to prototype solutions. It leverages an RPI 5 compute module to automate testing of the tiles or to assist in creating solutions.



Board Architecture

## The RPI 5 provides:

- **Processor:** At its core is the Broadcom BCM2712, a quad-core 64-bit Arm Cortex-A76 SoC clocked at 2.4 GHz. This is the same high-performance processor found in the Raspberry Pi 5, offering a substantial leap in computational power.
- **Memory:** The CM5 is available with LPDDR4X SDRAM in configurations of 2GB, 4GB, and 8GB, with 16GB variants expected in 2025, providing ample memory for demanding applications. ECC (Error-Correcting Code) support is also included for enhanced reliability.
- **Storage:** Onboard eMMC Flash storage options include 16GB, 32GB, and 64GB. A “Lite” version with 0GB eMMC is also available, allowing for external storage solutions via SD card or NVMe. 128GB eMMC variants are anticipated in 2025.
- **Graphics:** It features an 800 MHz VideoCore VII GPU, supporting OpenGL ES 3.1 and Vulkan 1.2, enabling robust multimedia and display capabilities.

### Connectivity:

- **Wireless (Optional):** Integrated 2.4 GHz / 5.0 GHz IEEE 802.11 b/g/n/ac Wi-Fi and Bluetooth 5.0, BLE, with an electronic switch for internal PCB trace or external antenna.
- **Ethernet:** Onboard Gigabit Ethernet PHY with IEEE 1588 support for precise time synchronization.
- **PCIe:** A 1x PCIe x1 Gen 2 root complex (5 Gbps), commonly used for high-speed peripherals like NVMe SSDs via an M.2 M-key socket on carrier boards
- **USB:** Two USB 3.0 ports (5 Gbps simultaneous operation) and one USB 2.0 port (high speed).
- **Video Interfaces:** Two HDMI 2.0 ports capable of simultaneously driving dual 4Kp60 displays.
- **Camera/Display Interfaces:** Two 4-lane MIPI ports, configurable for either DSI (display) or CSI-2 (camera).
- **General Purpose I/O (GPIO):** Up to 30 configurable GPIO pins, supporting 1.8V or 3.3V signaling, with a wide range of peripheral options including UART, I2C, SPI, SDIO, DPI, I2S, and PWM.

## The Nexus Carrier Board provides:

- Direct JTAG access to the tiles JTAG Pins
- USB JTAG access via USB C
- USB C Access to a FTDI 4232H mapped to the FPGA tile IO ring
- Skyworks clock generator connected to dedicated clock inputs on the FPGA Tile I/O ring. This is configurable using an external programmer or via the CM5
- Two Pmods connected to the FPGA tile I/O ring for interfacing with external peripherals
- USB C access directly to the FPGA pins to enable development of FPGA USB solutions
- USB C access to the RPI CM5 for configuration and set up
- GPIO connections between the FPGA Tile I/O ring and the RPI CM5
- Ethernet, WiFi, Bluetooth, 2 MIPI CSI/DSI interfaces, Dual HDMI and Dual USB A provided by the RPI CM5



The **Polaria Space Tile** provides developers with a compact way to integrate Linux-capable RISC-V processing and non-volatile FPGA acceleration without the complexity of designing a chip-down PolarFire SoC solution.



Built around the Microchip PolarFire SoC MPFS160, **Polaria** combines deterministic processing, reconfigurable logic and high-speed connectivity for onboard computing, payload processing and real-time data handling.

#### The tile measures 59 x 59mm and is built around:

- Microchip PolarFire SoC MPFS160TLS-FCVG784I
- Five-core, 64-bit RISC-V processor subsystem
  - Four SiFive U54 RV64GC application cores
  - One SiFive E51 RV64IMAC monitor core
- Processor operation up to 667 MHz
- 2 MB configurable L2 cache, scratchpad or loosely integrated memory
- 161K non-volatile FPGA logic elements
- 498 × 18-bit by 18-bit multiply-accumulate blocks
- 11.3 Mbit of embedded FPGA memory
- 415 Kbit embedded µPROM
- Eight PLLs and eight DLLs
- 128 Kbyte embedded non-volatile boot memory
- Secure non-volatile memory and hardware root-of-trust capabilities
- Instant-on, non-volatile FPGA configuration
- FCVG784 package, 23 × 23 mm with 0.8 mm pitch
- Pin-compatible migration path to the RTPFS160ZT radiation-tolerant device

## Interfacing:

- Eight high-speed SerDes lanes operating from 250 Mbps to 12.7 Gbps
- Two integrated PCIe Gen2 controllers
  - Root-port or endpoint operation
  - ×1, ×2 and ×4 lane configurations
- Two Gigabit Ethernet MACs
- Two CAN 2.0A/B controllers
- One USB 2.0 OTG controller
- MMC 5.1, SD and SDIO controller
- Execute-in-place QSPI flash controller
- Five multi-mode UARTs
- Two SPI controllers
- Two I<sup>2</sup>C controllers
- RTC, GPIO, timers and five watchdog timers
- Integrated DDR3, DDR4, LPDDR3 and LPDDR4 memory controller with optional SECDED
- Three 64-bit AXI4 interfaces between the processor subsystem and FPGA fabric
- One 32-bit APB interface between the processor subsystem and FPGA fabric
- Up to 136 processor-subsystem I/O, 144 high-speed I/O and 168 FPGA GPIO connections available in the selected package

## Supported development ecosystem

Polaria development is supported by Microchip's established PolarFire SoC ecosystem, including:

- Libero SoC Design Suite for FPGA development
- SoftConsole embedded software development environment
- PolarFire SoC MSS Configurator
- Mi-V RISC-V development ecosystem
- Hart Software Services boot and platform-management firmware
- Linux, RTOS, asymmetric multiprocessing and bare-metal deployment
- SmartDebug processor and FPGA debugging
- FlashPro Express programming tools
- PolarFire SoC Icicle Kit and Discovery Kit reference platforms
- VectorBlox Accelerator SDK and CoreVectorBlox neural-network accelerator IP

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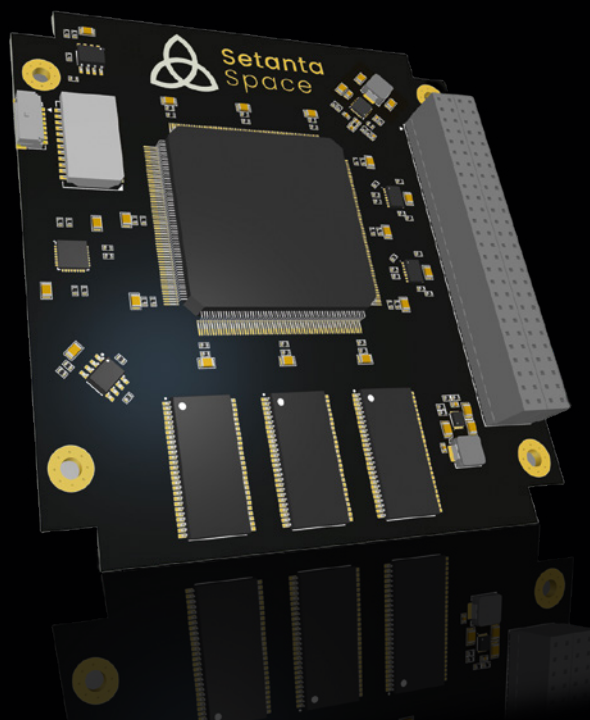
## Typical applications which would benefit from the tile:

- **Payload processing**, real-time filtering, transformation and management of payload data
- **Image and signal processing**, FPGA acceleration of deterministic processing pipelines
- **Onboard AI**, hardware-assisted inference and preprocessing
- **Protocol conversion**, bridging between processor, FPGA and high-speed serial interfaces
- **Sensor aggregation**, collecting and preprocessing multiple data sources
- **High-speed data routing**, using PCIe, Ethernet and multi-gigabit transceivers
- **Secure onboard computing**, authenticated boot, protected key storage and anti-tamper functions
- **Fault monitoring**, watchdog, error-correction and FPGA-based supervision
- **Linux application hosting**, deployment of higher-level onboard software alongside deterministic FPGA logic
- **Rapid prototyping**, development on commercial PolarFire SoC hardware with a pathway to radiation-tolerant silicon



**Dagda** is a high-performance onboard computing platform designed for spacecraft AI, payload processing, computer vision, and autonomous operations.

Built around a resilient **Microchip PolarFire SoC MPFS460TLS** control layer and modular **Space Tile+** accelerators, **Dagda** combines deterministic spacecraft interfacing with GPUs, NPUs, FPGAs, and adaptive compute devices.



### Key features

- Heterogeneous onboard computing architecture
- MPFS460TLS PolarFire SoC control and management layer
- Modular Space Tile+ accelerator ecosystem
- Support for GPUs, NPUs, and FPGAs
- High-speed PCIe accelerator connectivity
- Linux-based heterogeneous workload management
- Designed for AI, autonomy, and payload processing

## System Architecture

### Control and Management Layer

- **Device:** Microchip PolarFire SoC MPFS460TLS-FCG1152I
- Five-core, 64-bit RISC-V processor subsystem
- 461K-element non-volatile FPGA fabric
- Accelerator supervision and reset control
- Spacecraft communications and data routing
- Power sequencing and health monitoring
- Fault detection, isolation, and recovery
- Independent deterministic control plane

The PolarFire SoC remains operational independently of the main accelerator, allowing DAGDA to monitor, isolate, and recover high-performance compute devices.

### Space Tile+ Concept

- Standardised, replaceable accelerator modules
- Supports GPUs, NPUs, FPGAs, and adaptive compute devices
- Integrates processing, memory, storage, power, and high-speed interfaces
- Allows accelerators to be selected for mission power, latency, and throughput needs
- Reduces redesign and integration effort
- Enables future processor upgrades without replacing the full platform

### Example Space Tile+ modules

- NVIDIA GPU
- M.2 NPU and VPU modules
- AMD Versal adaptive compute
- Mission-specific FPGA or payload processor

## Variants

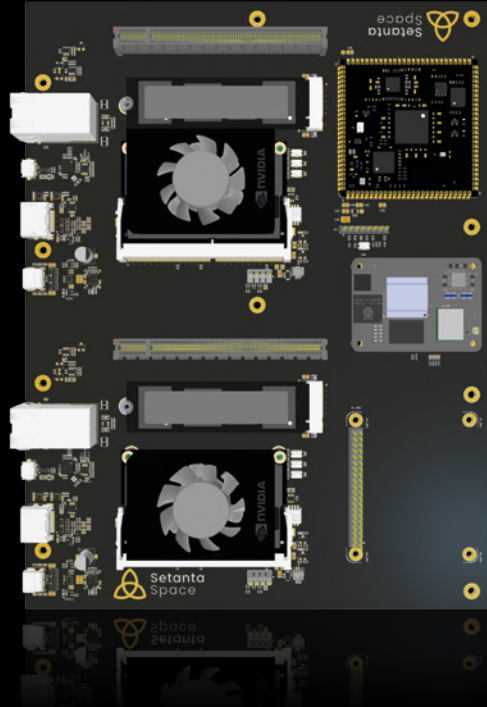
### Dagda RT

- Planned **RTPFS460ZTLS-based** radiation-tolerant configuration
- Radiation-tolerant control and spacecraft-interface layer
- Accelerator isolation, reset, and fault recovery
- Intended for longer-duration and higher-reliability missions

Radiation performance will depend on the selected accelerator, memory, storage, shielding, and mission environment.

## Applications

- Onboard AI inference
- Computer vision and image processing
- Earth observation processing
- Optical navigation
- Space situational awareness
- Autonomous spacecraft operations
- Payload data handling
- Sensor fusion
- Data compression and prioritisation
- Defence and intelligence missions



**Ogma** is a sandbox platform for deploying and benchmarking edge AI. It offers a broad catalog of compute architectures, from conventional CPUs to next-generation accelerators, exposed through a single, unified interface.

A Raspberry Pi Compute Module serves as the primary control and interface board, providing connectivity to two NVIDIA SO-DIMM connectors, two PCIe slots, and two M.2 slots.

**Ogma can host a wide range of devices, including but not limited to:**

- Setanta Space Tiles
- NVIDIA Jetson Orin Nano
- NVIDIA Jetson Orin NX
- Axelera Metis
- Hailo variants
- BrainChip variants
- FPGA modules

The platform enables real-time comparison of algorithm and pipeline performance on state-of-the-art edge hardware, including power consumption, supporting the identification of the most suitable hardware for your model, pipeline, and mission.

# Tiles in development

## Stellaria

An edge-AI-optimized FPGA module combining a Lattice FPGA with integrated BrainChip Akida® neuromorphic IP accelerator to deliver ultra-low-power, fault-tolerant AI inferencing and event-driven processing for real-time decision making, anomaly detection, and autonomous operations at the spacecraft edge.

## Singularia

A high-capacity, radiation-tolerant mass-memory tile designed to provide reliable, high-throughput data storage for space missions, enabling the buffering, retention and management of large volumes of payload, sensor and AI-generated data in harsh environments, with an architecture optimised for fault tolerance, data integrity and deterministic access patterns, making it ideal for onboard data recording, AI dataset caching, autonomous mission operations and delayed downlink scenarios in satellite and deep-space systems (leveraging space-qualified memory technologies, robust error detection and correction, and a modular interface compatible with the Space Tile ecosystem for scalable, mission-specific storage configurations).

# AI Solutions

## Treating Explainability as a critical need in space beyond diagnostic validation

Explainability is embedded across the AI lifecycle, from data curation and training, through onboard inference, to post-decision analysis and continuous improvement, ensuring that autonomous systems remain transparent, auditable, and aligned with human operational intent.

Our approach recognises that mission-critical AI must support:

- Operator trust and accountability
- Rapid fault isolation and recovery
- Robust autonomy under uncertainty
- Continuous learning without loss of safety margins

Rather than relying on a single explanation technique, Setanta Space integrates layered XAI mechanisms throughout the model stack. These layers operate at different abstraction levels, enabling both machine-level verification and human-level understanding.

## Human-in-the-loop feedback as a control signal

Setanta Space integrates layered explainability and human-in-the-loop feedback directly into the AI lifecycle, enabling explanations generated on board or during ground analysis to be reviewed, corrected, and reintegrated as supervisory signals. This approach ensures that autonomous systems remain verifiable, correctable, and aligned with operator intent and domain knowledge across all mission phases, transforming explainability from a passive diagnostic into an active control signal that improves robustness, reduces operational risk, and enables long-duration, communication-limited autonomy.

This enables spacecraft AI systems to:

- Continuously improve through explainability-guided retraining and fine-tuning
- Reduce recurring false positives and brittle behaviours via targeted feedback
- Feed operational insight directly back into model updates across missions
- Justify decisions transparently under uncertainty and degraded conditions
- Deliver deployable, defensible, and mission-ready autonomy across all AI capabilities



## Onboard anomaly detection and FDIR

Real-time spacecraft health monitoring with autonomous fault detection, isolation, and recovery to increase mission reliability and reduce ground intervention.

## Swarm and constellation coordination

Distributed AI across multiple spacecraft, enabling cooperative processing, redundancy, and intelligent constellation-level behavior.

## Space Situational Awareness

Real-time detection and assessment of nearby spacecraft and debris to improve collision avoidance and operational safety.

## Agentic AI

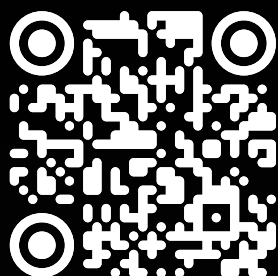
Agentic satellite intelligence with autonomous agents that ingest, reason over, and act on geospatial data streams to enable adaptive tasking, anomaly response, and continuous, decision-driven operations with minimal ground intervention.

## Autonomous navigation

Onboard guidance and decision-making that enables spacecraft to navigate, maneuver, and operate independently in communication-limited environments.

## Real-time Earth observation analytics

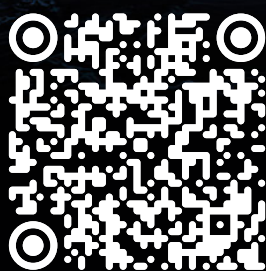
Onboard AI for change detection, ship detection, and environmental monitoring, reducing downlink needs by transmitting only mission-critical insights.



Visit [setantaspace.com](https://setantaspace.com)

or email

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See our products in action at

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