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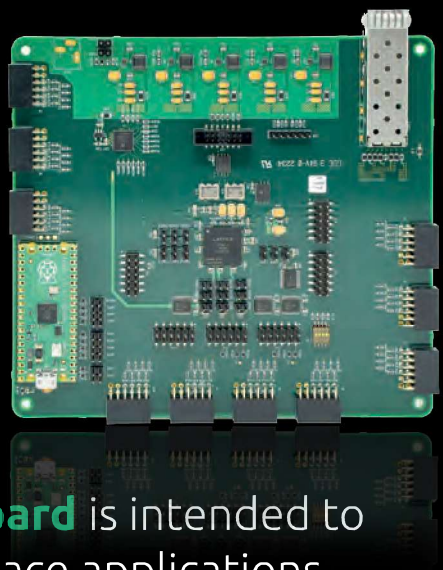
DEVELOPMENT BOARD



The **Galaxia® Space Development Board** is intended to support development of demanding space applications, which require low power, high performance and of course a low single event upset rate.

It provides users with a Certus™-NX LFD2NX-40 which is the commercial equivalent of the Certus-NX-RT device offered by CAES, and is an excellent platform for the development of applications including:

- Deployment Cameras
- Temperature Control Systems
- Motor and Actuator Control
- Telemetry and Telecommand processing
- Health and Usage Monitoring
- Radiation Beam Testing for design proving
- Implementing Compression algorithms
- Implementing Cryptographic security

The board provides users with:

- Certus™-NX LFD2NX-40
- 80 I/O accessible via Pmod
- 14 ADC Channels – Including ADC Reference
- 128 Mbit NOR flash for configuration
- 256 Kbit MRAM memory
- 100 MHz Oscillator
- Lattice In-System Programmable Hardware Management Expander
- RPi Pico

The Lattice Certus™-NX FPGA provides the user with 40K LUTs, 2.5 Mbit of BRAM, 56 DSP (18x18), two ADCs and inbuilt 32 KHz and 450 MHz Oscillators.

Further capabilities

It is also possible to deploy RISC-V processors on this development board, using the Lattice Propel tool. Examples of this can be examined in the tutorials at adiuvoengineering.com/post/lattice-propel-risc-v-part-one-hardware and adiuvoengineering.com/post/lattice-propel-risc-v-part-two-software-development.

What makes the Galaxia® Space Development Board unique is the provision of the RPi Pico, providing developers with a wide range of capabilities including:

- **Clock Generation** – Generation of up to 65 MHz reference clock using the PIO.
- **Communications emulation** – Emulation of a differential backplane bus.
- Communications Monitoring – Monitoring and logging communications.
- **Sensor emulation** – Emulation of sensors across the system and implementation of failure modes.
- **Complex communications creation** – Implementation of a space wire communication protocol between the FPGA and the Pico. This provides a simple interface which can be controlled over the USB communication.
- **Power management and monitoring** – Monitoring the power network, to control, monitor and observe the dissipated power as the FPGA design is used under load or to test, for example, a beam line.

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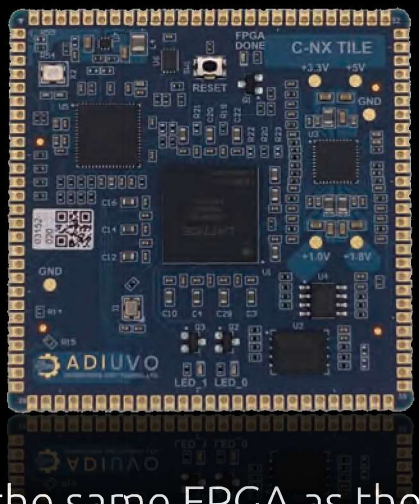
SPACE TILE



The **Galaxia® Tile** is developed using the same FPGA as the Galaxia® Development Board, enabling it to be designed into missions or more advanced prototyping/testing solutions.

The tile measures 59mm x 59mm and provides developers with:

- Single Supply Voltage 4.5V to 18V
- Onboard UART Debug Interface
- Lattice Certus™-NX LFD2NX-40
- Configuration Memory 256 Mbit QSPI
- Done LED and Two user LEDs
- USB JTAG
- USB Connector needed on carrier board
- 100 MHz Oscillator
- Other Global clock pins broken out via I/O
- Reset Button
- PSRAM – 32 Mbit – Serial RAM connected to the FPGA
- 82 I/O including – Power and Ground, JTAG, 32 I/O at 3v3, 41 I/O configurable voltage (3v3-1.2V and LVDS)