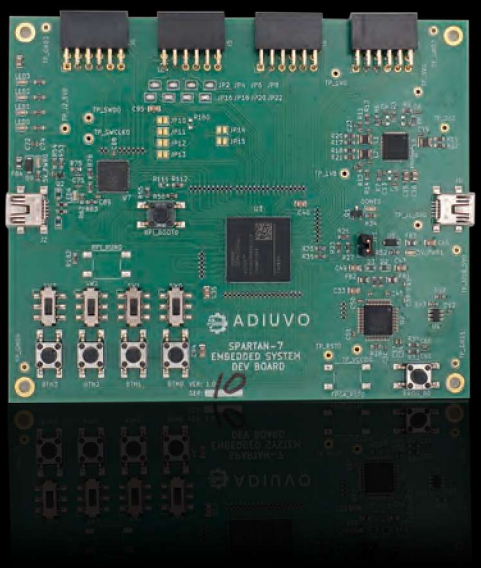
astria BOARD

The **Astria & RPI 2040** is designed to support a range of developments from simple logic and embedded system development, to more complex solutions such as image processing.



Key features

- AMD Spartan 7 XC7S6 with 6,000 logic cells, 5 BRAM, 2 CMT, 10 DSP48
- Raspberry PI RP2040 processor providing dual-core Arm Cortex-M0+ processor running at 133 MHz
- FTDI232H - For JTAG Programming
- SDRAM - 64 Mbit
- 4 Pmod - Three for FPGA, one for RPi 2040 - Ability to fit high speed LVDS transceiver on one FPGA Pmod
- User Flash - connected to FPGA 32 Mbit QSPI
- FPGA Configuration PROM 256MBit
- Four User LEDs
- Four push button switches
- Four SPST switches
- 100 MHz Reference clock

Application examples include:

- **RPI_FPGA_UART_AXI** *Vivado 2023.2* Configures a UART in the RP2040 to communicate with the FPGA, sending a protocol over the UART and IP in the FPGA AXI peripherals can be accessed and controlled. In this version three AXI GPIO are connected to three LEDS, the final LED is connected to an AXI timer to demonstrate PWM on the LED. The 4 slide switches are also connected to the AXI GPIO to enable their status to be read over the AXI GPIO.
- **SDRAM** *Vivado 2023.2* - SDRAM example for the SDRAM on the board.
- **MBV_MCS** *Vivado & Vitis 2024.1* MicroBlaze V (RISC-V) MicroController System implemented on the Spartan 7.
- **S7_LEO** *Vivado 2023.2* IO check of all FPGA PMOD IO and 4 LED, walks an LED around all 28 LEDS (4 on board, 24 on Pmod LED - not included) - also connects through the user flash to the RPI for testing.
- **DELTA_SIGMA** *Vivado 2024.1* Delta Sigma output at 1KHz on PMod 1 pin 1, PWM sine output at 1 KHz on Pmod 1 pin 2 - external RC needed for recovery.

References

Reference Designs, XDC, Schematics, Vivado board definition can be found at
https://bitbucket.org/adiuvo-engineering/leonidas_embedded_development/src/main/

astria TILE

The **Astria Embedded System Tile** provides developers with a risk-free way of integrating a Spartan 7 in their design without the worry of designing a chip-down solution.

The tile measures 59 x 59mm and provides:

- Supply voltage 4.5 to 18V
- Spartan 7 XC7S25 with 23,360 Logic Cells, 80 DSP, 45 BRAM
- Configuration Memory 256 Mbit QSPI
- Done LED
- Two user LED
- USB JTAG - Connector needed on carrier board
- 100 MHz Oscillator
- Reset Button
- Boot selection header (JTAG/QSPI)
- PSRAM – 32 Mbit – Serial RAM connected to the FPGA
- 82 I/O including – Power and Ground, JTAG, 32 I/O at 3v3, 41 I/O configurable voltage (3v3-1.2V and LVDS)

To help get you started, the Astria Embedded System Tile comes with:

- User guide
- Schematic
- Vivado Board definition
- Reference Designs - including IP to enable processor to access FPGA internals using processor UART / SPI
- Tile footprint in Altium to help accelerate your design

This information is presented on Adiuvo Engineering's public repository and Setanta Space can be contracted to develop your application or assist with it.

Typical applications which would benefit from the tile:

- **System Controller** – Power supply sequencing, power monitoring, configuration management, board management and supervision / communication interface.
- **Protocol conversion** – Convert to and from bespoke / legacy protocol.
- Sensor Aggregation **–** Aggregate several different sensor types for easy access by processor
- **I/O expansion** – Provide additional interfaces e.g. QSPI, SPI, I2C etc.
- **Processing offloading** – e.g. Control algorithm such as PID, Filtering, co-processing , encryption / decryption of data streams entering and leaving system.
- **Health and Usage Monitoring systems** – Integrate with sensors e.g. accelerometer, pressure, humidity etc to monitor the environmental operating conditions.
- **Rapid Prototyping** – quickly demonstrate the concept required in an FPGA. Reduces risk of FPGA integration / Removes obsolescence management issues.